AMENDMENT TO CLAIMS

Please **AMEND** claim 1.

No new matter has been added. This listing of claims will replace all prior versions, and listings, of claims in the application:

In the Claims

A copy of all pending claims and a status of the claims is provided below.

1. (Currently amended) A semiconductor structure formed on a substrate, comprising at least one of an n- FET device and a p-FET device, a shallow trench isolation having at least one overhang is selectively configured to prevent oxidation induced stress in a determined portion of the substrate, and wherein the at least one overhang is selectively configured to prevent oxidation induced stress in at least one of a direction parallel to and transverse to a direction of a current flow, wherein:

for the n-FET device, the at least one overhang is selectively arranged in directions of and transverse to a current flow, and

for the p-FET device, the at least one overhang is arranged transverse to the current flow to prevent performance degradation from compressive stresses.

2. – 3. (Canceled)

4. (Previously Presented) The semiconductor structure of claim 1, wherein:

the determined portion of the substrate is an Si-SiO_2 interface adjacent to the shallow trench isolation; and

the at least one overhang extends beyond the Si-SiO_2 interface, preventing oxidation at or near the Si-SiO_2 interface.

5. (Previously Presented) The semiconductor structure of claim 1, further comprising:

the n-FET device having a source and a drain with a direction of current flow for the n-FET device; and

the p-FET device having a source and drain with a direction of current flow for the p-FET device;

wherein the shallow trench isolation includes:

a first shallow trench isolation side for the n-FET device having at least one overhang configured to prevent oxidation induced stress in a direction parallel to the direction of current flow for the n-FET device; and

a second shallow trench isolation side for the n-FET device having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the n-FET device; and

a third shallow trench isolation side for the p-FET device having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the n-FET device.

6. (Previously Presented) The semiconductor structure of claim 5, wherein the shallow trench isolation further includes a fourth shallow trench isolation side for the p-FET

device, the fourth shallow trench isolation being devoid of an overhang.

7. (Original) A semiconductor structure formed on a substrate, comprising:

an n-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain; and

a first shallow trench isolation for the n-channel field effect transistor, the first shallow trench isolation having a first shallow trench isolation side, the first shallow trench isolation side having at least one overhang configured to prevent oxidation induced stress in a direction parallel to the direction of current flow for the n-channel field effect transistor.

8. (Original) The semiconductor structure of claim 7, wherein the first shallow trench isolation for the n-channel field effect transistor further comprises:

a second shallow trench isolation side being transverse to the first shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the n-channel field effect transistor.

9. (Original) The semiconductor structure of claim 8, further comprising:

a p-channel field effect transistor, the p-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain;

a second shallow trench isolation for the p-channel field effect transistor having a third shallow trench isolation side, the third shallow trench isolation side being devoid of an overhang; and

the second shallow trench isolation for the p-channel field effect transistor further having a fourth shallow trench isolation side, the fourth shallow trench isolation side being transverse to the third shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the p-channel field effect transistor.

10. (Original) The semiconductor structure of claim 9, wherein the overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow prevents a degradation of hole mobility.

11. (Original) The semiconductor structure of claim 9, wherein:

the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the first shallow trench isolation would affect performance of the n-channel field effect transistor, and

the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the second shallow trench isolation would affect performance of the n-channel field effect transistor.

12. (Original) The semiconductor structure of claim 1, wherein the overhang includes a T-shaped structure.

13. (Previously Presented) The semiconductor structure of claim 12, wherein the determined portion of the substrate is an Si-SiO_2 interface adjacent to the shallow trench isolation.

14. (Previously Presented) The semiconductor structure of claim 13, wherein the overhang includes a horizontal portion that extends beyond the Si-SiO_2 interface by about 0.01 microns to 0.5 microns.

15. (Original) The semiconductor structure of claim 9, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side for the second shallow trench isolation for the p-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the fourth shallow trench isolation side would affect performance of the p-channel field effect transistor.

16. (Original) The semiconductor structure of claim 15, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side is less than or equal to about 5.0 microns.

17. (Original) The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side is less than or equal to about 5.0 microns.

18. (Previously Presented) The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side is less than or equal to about 5.0 microns.

19. – 22. (Canceled)